K-2

GaAs FET LINEAR POWER AMPLIFIERS FOR 16 QAM SIGNALS AT 6 AND 11 GHz

A. Barzaghi, F. Oggionni, G. Pratesi
Microwave Communication Labs,
Telettra SpA - Vimercate (MI), Italy

ABSTRACT

This paper describes design and realisation criteria for linear power amplifiers used in novel 16 QAM radio link systems. The 6.4-7.1 GHz amplifiers use 6 cascaded stages and perform a .9 W mean output power with a 42 dB linear gain and -37 dBc 3rd order IM. The 10.7-11.7 GHz version uses 8 cascaded stages to perform a .5 W mean output power with the same distortion value.

Introduction

GaAs FET represents the only available solid state solution to perform power amplification at frequencies higher than 4 GHz with the linearity value required for 16 QAM signals.
Many high power GaAs FET amplifiers for TWT replacement have been reported (1, 2, 3), but only a few specific works for linear power amplifiers suitable for 16 QAM signals have been represented (4).
The following paper outlines design and realisation criteria of linear power amplifiers, used in 140 Mbit/s 16 QAM radio link systems at 6 and 11 GHz. Particular considerations are given for:

- amplifier linearity performances versus RF and DC GaAs FET operating point;
- linearity performances with devices of various manufacturers;
- temperature evaluations of GaAs FET channels;
- linearity improvement by adoption of a pre-distortion circuit and comparison with TWT amplifier characteristics;
- BER performances of an amplifier inserted in a complete 140 Mbit/s radio link.

Amplifier structure

Figs.1 and 2 give block diagrams for 6.4-7.1 and 10.7-11.7 GHz amplifiers with fundamental signal levels and 3rd IM values for the cascaded stages.
Stability of the linear gain versus temperature and versus device characteristics spreading is ensured by an ALC loop. The output detector is optimized to give a voltage proportional to the mean value of the RF signal, in order to avoid that ALC operating depends on the amplitude modulation index of the RF signal (fig.3).
All GaAs FETs are provided with a hermetic package. The microwave microstrip circuits are realised on a duroid substrate, while the bias networks use the thick-film technology.
The input variable attenuator uses two PIN diodes driven by the ALC loop and mounted in a balanced structure (fig.4).
The cooling fins (H = 35 mm) and the amplifier box are made of a unique piece of aluminium (H=528, W=110, D=78 mm) thus optimizing the heat flow from the power devices flanges towards the ambient (fig.5). The maximum overtemperature of the final GaAs FET flanges is 22°C while the highest channel temperature is 130°C.

Design criteria

Main targets to perform in designing linear power amplifiers may be summarised as follows:

i) obtaining stable linear operation versus temperature and versus GaAs FET characteristics spreading;
ii) operating with the lowest possible back-off value with respect to saturation, in order to reduce cost and channel temperature of the power devices.

Considering these targets the following design criteria may be pointed out:

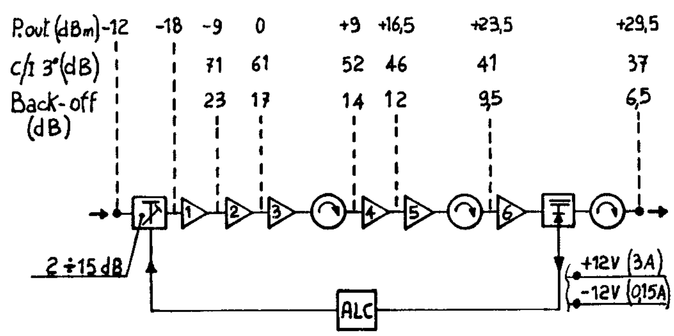


Fig. 1 - Block diagram of the 6.4-7.1 GHz amplifier

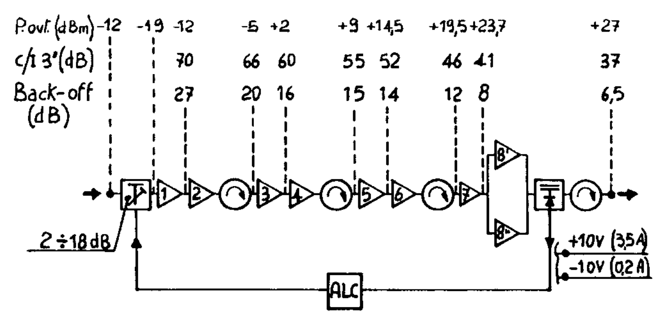


Fig. 2 - Block diagram of the 10.7-11.7 GHz amplifier

DC operating point

For optimum linear operation the bias current is 10 to 15% lower than IDSS/2, while the bias voltage is 5-10% higher with respect to the standard value.
Being the source directly grounded, both positive and negative bias voltages are requested.
Furthermore a proper DC control loop circuit for each device is used.
This circuit provides constant ID operation versus temperature and versus device characteristics spreading.
Constant ID operation has been preferred over constant VGS operation to obtain a better control of GaAs FET channel temperature.

RF operating point

The back-off value with respect to the saturated output power is the most important factor influencing the amplifier distortion.
On the other hand the higher is the back-off, the higher is the dissipated power for the device. For these reasons the back-off value for the cascaded stages passes from 23 to 17 dB in the low level stages, where no particular problems exist for device channel temperature, up to 6.5 dB for the final stages in order to obtain the required output power and linearity values with the lowest possible saturated output power of the final device.
This distribution of back-off values finally results in a lower cost for the GaAs FET kit and a lower DC power supply for the complete amplifier.

Matching networks

The matching conditions required for linear operation are similar but not exactly equal to the maximum gain conditions. Therefore matching networks are computer designed for maximum gain condition. After that linearity optimisation is obtained by means of a small adjustment on that network.

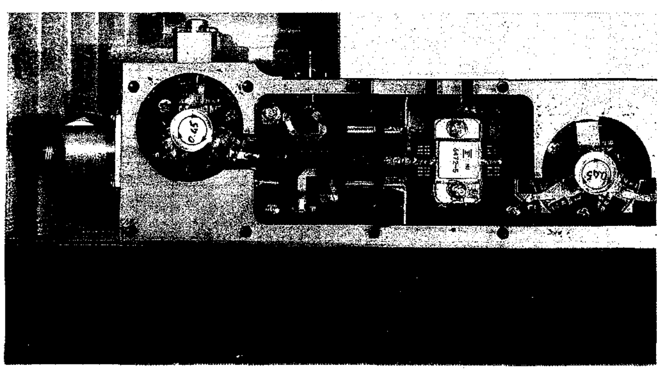


Fig. 3 - The final stage of 6.7 GHz amplifier

Performances

The instantaneous band coverage of each amplifier is 5% with an amplitude flatness of .2 dB on 60 MHz bandwidth.
Fig.6 reports the output amplitude variations versus temperature.

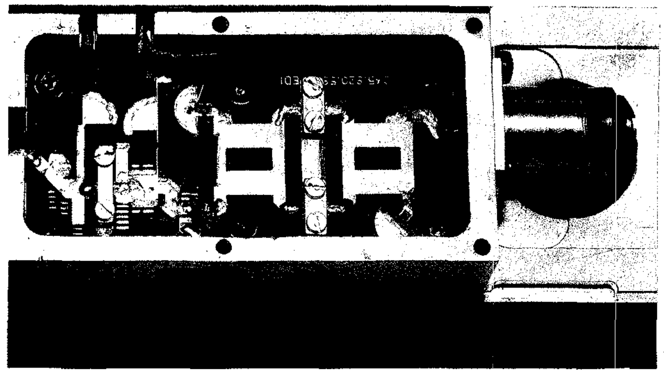


Fig. 4 - The input variable attenuator at 6.7 GHz

In fig.7 output power, 3rd order IM and 5th order IM values are given versus the input signal level for the 6.7 GHz amplifier.
The 3rd IM and 5th IM plots do not only depend on the device characteristics but also on the operating frequency that influences phase of IM products.
In fig.8 BER performances of the amplifier inserted in a 6.7 GHz 140 Mbit/s radio link are given.
Using the predistortion technique the mean output power of GaAs FET amplifier for 37 dB 0 to 45°C third-order distortion has been increased by 1.5 dB, reducing the final stage back-off to 5 dB.
Performances compared with a high efficiency TWT amplifier, are given in table 1 for 6.7 GHz.
While the TWT presents a dominant 3rd order distortion, the GaAs FET has also a consistent 5th order distortion not compensated by the predistortion circuit and that limits the compensation amount of the 3rd order distortion.

Table 1

3rd order predistortion technique performances for GaAs FET and TWT amplifiers.
Distortions are measured at 25°C, while in parenthesis values in the 0 to 45°C temperature range are reported.

C/I (dB)	GaAs FET amp out pow (dBm) Psat = +36 Pmean = +31		High eff TWT amp out pow (dBm) Psat = +41.5 Pmean = +33	
	third order	fifth order	third order	fifth order
without pre-distortion	32	44	30	50
with third order pre-distortion	42 (37)	42 (40)	45 (40)	48 (46)

Acknowledgements

The authors wish to thank Mr. L. Vismara for his contributions to measurements and valuable discussions.

References

1) Y.Arai, S.Murai and H.Komizo
A 4 GHz TWT replaceable GaAs amplifier
Proc. 8th Europ. Microw. Conf. - Paris 1978
2) Y.Arai, S.Murai and T.Sakane
High power GaAs FET amplifier for TWT replacement
Fujitsu Sc. and Tech. Journal - Vol.15 n°3 1979
3) H.Komizo, et al
A 7 GHz FM transmission utilizing GaAs power MESFET, - International Microwave Symposium - 1977 IEEE-MTT-S
4) Radio repeater design for 16 QAM by Schwarz and others - IEEE ICC - 1981

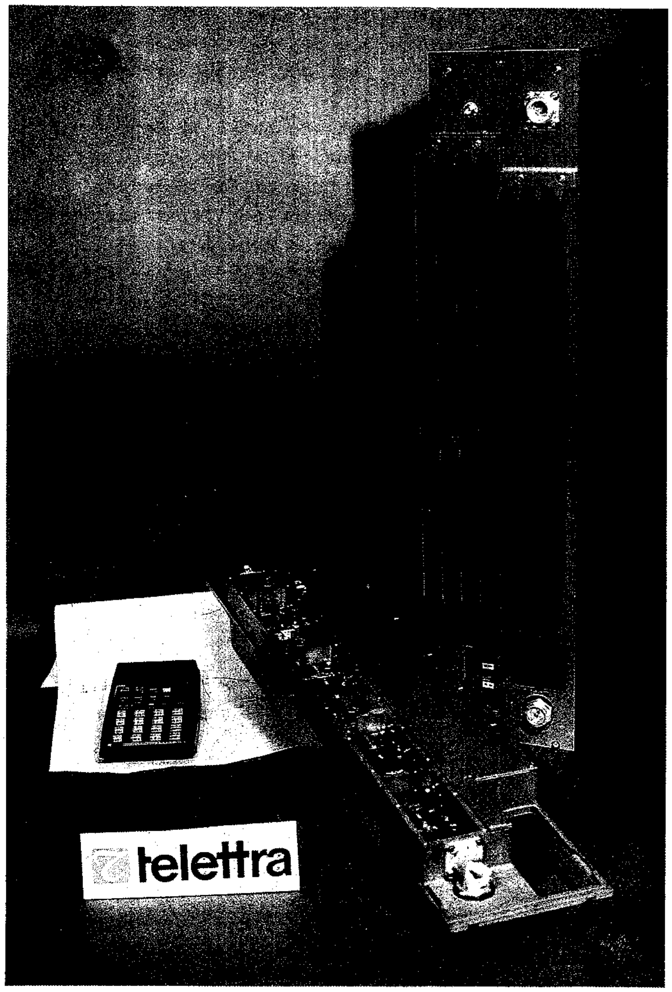


Fig. 5 - The complete 6.4-7.1 GHz linear amplifier

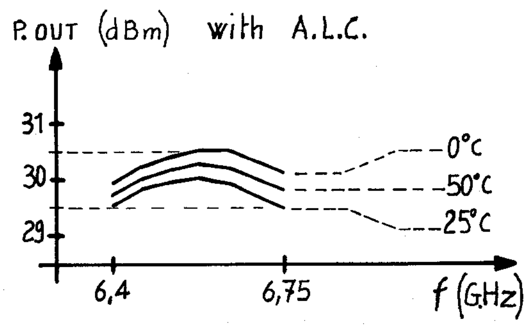
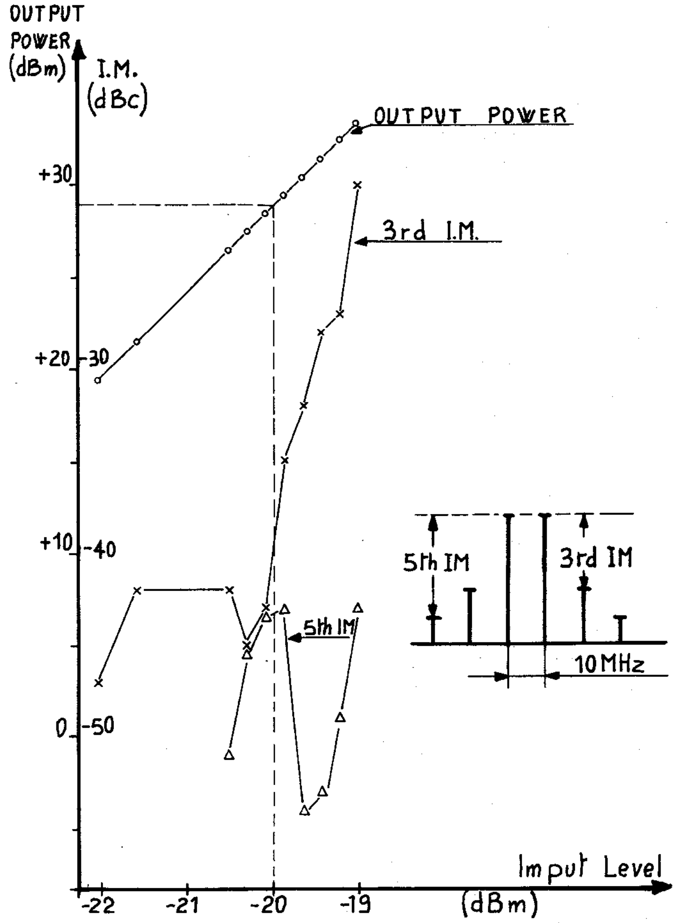


Fig. 6



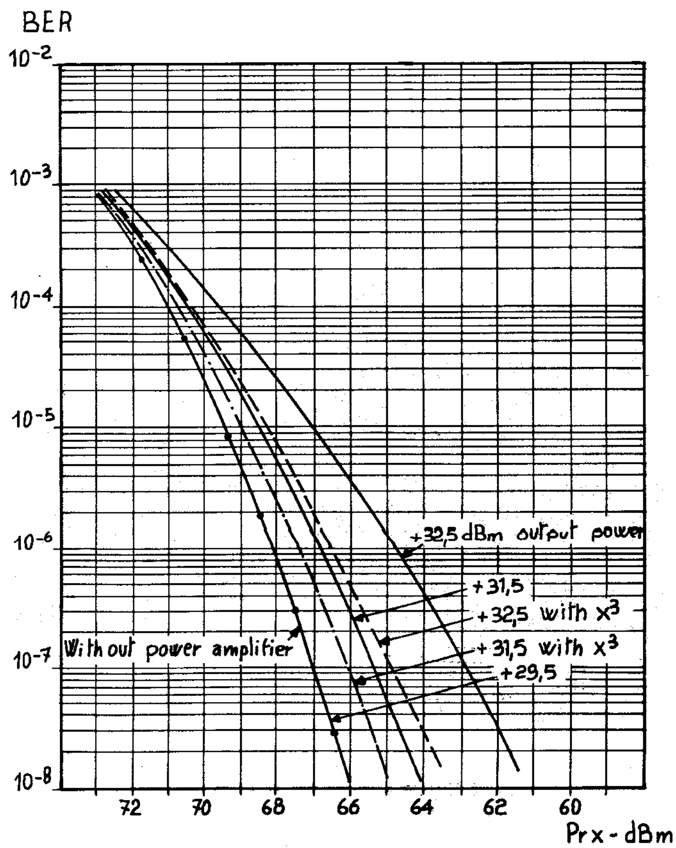


Fig. 8 - BER characteristics